REMARKS

A complete listing of all the claims in the application is shown above showing the status of each claim. For current amendments, inserted material is underlined and deleted material has a line therethrough.

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

Claims 31, 34 and 40 are currently amended.

Claims 1-20, 33 and 37 are now canceled.

No new matter has been added.

Allowable Subject Matter

Applicants appreciate the allowance of claims 21-30.

The Examiner has also indicated that claims 33, 34 and 40 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, applicants have amended base claim 31 by adding the limitations of now canceled claim 33 thereto, and have amended the dependency of claim 34. Applicants have also included the limitations of base claim 31 into now independent claim 40. In view of the foregoing, it is submitted that claims 31, 32 and 34-40 are now in a condition for allowance.

The Examiner has also requested the non-patent literature/other art that was filed as part of the IDS of 11/25/2003. Accordingly, applicants are submitting herewith copies of such non-patent literature as identified below:

"A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", U. Gruening et al., IEDM 99-25, 1999.

"Extending Trench DRAM Technology to 0.15μm Groundrule and Beyond", T. Rupp et al., IEDM 99-33, 1999.

"A 0.135 μm^2 $6F^2$ Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", C. J. Radens et al., 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 80-81, IEEE, 2000.

In view of the foregoing, applicants respectfully submit that the application is in a condition where allowance of the case is proper. Reconsideration and issuance of a Notice of Allowance are respectfully solicited. Should the Examiner not find the claims to be allowable, Applicants' attorney respectfully requests that the Examiner call the undersigned to clarify any issue and/or to place the case in condition for allowance.

Respectfully submitted,

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A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb

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Abstract

Results are presented for a novel trench capacitor DRAM cell using a vertical access transistor along the storage trench sidewall which effectively decouples the gate length from the lithographic groundrule. A unique feature of this cell is the vertical access transistor in the array which is self-aligned to the buried strap [1] connection of the storage trench (VERI BEST) and bounded by trench isolation oxide. The VERI BEST cell concept, process and electrical results obtained from $8F^2$ test cell arrays at 0.175µm groundrules are described in this paper.

Introduction

With each new generation the available space for the channel length of the DRAM transfer device continues to shrink aggressively. Conventional scaling techniques are limited by the stringent leakage requirements of a DRAM cell as shown in Fig. 1: A reduction in gate poly length requires thinner gate oxides and increased channel doping to avoid short channel effects. High doping levels, however, lead to increased junction leakage which decreases data retention time [2]. At the same time gate oxide reliability requires reduction of the wordline voltage, thus degrading the charge writeback characteristics and signal margin, as the array threshold voltage remains fixed due to off-current requirements. Therefore a vertical array transistor is proposed as a means to decouple the gate length from the shrink path.

The proposed VERI BEST process is based on the advanced BEST [3] cell technology with a planar array transistor and raised shallow trench isolation [4] and a vertical pass transistor along the deep trench sidewall [5]. Cross-sectional views in Fig. 2 show the evolution from a conventional $8F^2$ planar MOSFET cell to the VERI BEST cell, as well as a

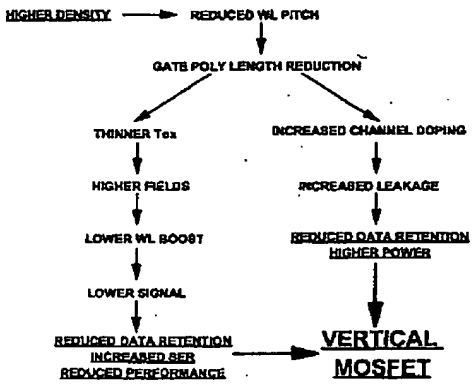

Fig. 1: Motivation for vertical access MOSFET for DRAM scalability.

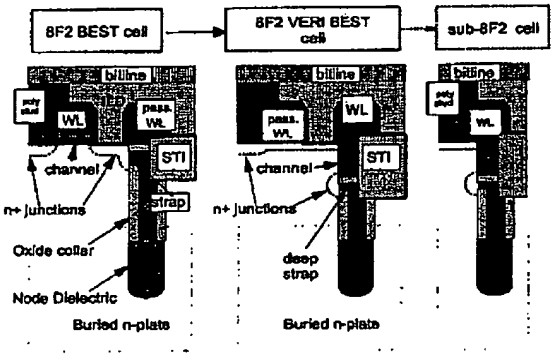

Fig. 2: Evolution from a planar $8F^2$ to vertical MOSFET cells:
(a) State-of-the-art $8F^2$ DRAM with planar channel. (b) Novel $8F^2$ DRAM cell with a vertical transistor channel on top of the deep trench storage capacitor (c) Potential shrink path to sub-$8F^2$ cells.

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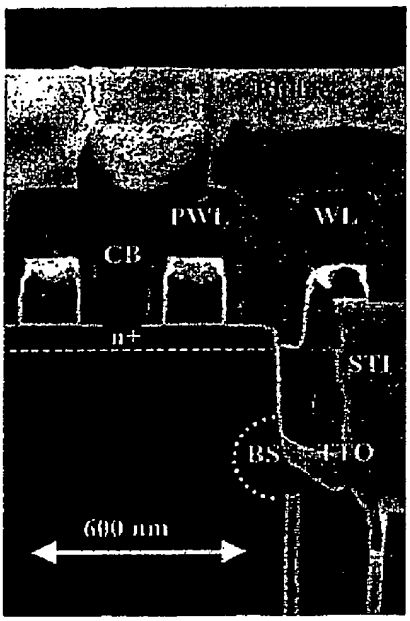

Fig. 3: SEM picture of $8F^2$ VERI BEST cell with vertical transistor, showing same X-sectional view as sketched in Fig. 2

potential shrink path to sub-$8F^2$ cells. From an addressing point of view, the two $8F^2$ cells are transformed into each other by exchanging logically the role of the active and passing wordlines (WL). The vertical transistor is now controlled by the formerly passing WL running across the top of the deep trench, its channel length being determined by the depth of a recess etch which can be optimized independently of the groundrule. Fig. 3 shows a SEM picture of the fabricated structure.

Process Flow

Fig. 4 shows schematically the process flow, as summarized in Table I. After forming the deep storage trench capacitor, the poly recess etch determining the buried strap depth is extended by about 0.3-0.4µm in order to accommodate space for the vertical transistor, followed by collar oxide removal and buried strap formation (Fig. 4a). The buried strap polysilicon is then covered with a trench top oxide (TTO) layer to insulate the node from the vertical gate poly and the pad layers are stripped. After implanting the wells for the array and support devices and the array n+-bitline junction, a gate oxide is grown (Fig. 4b) both at the planar surface and

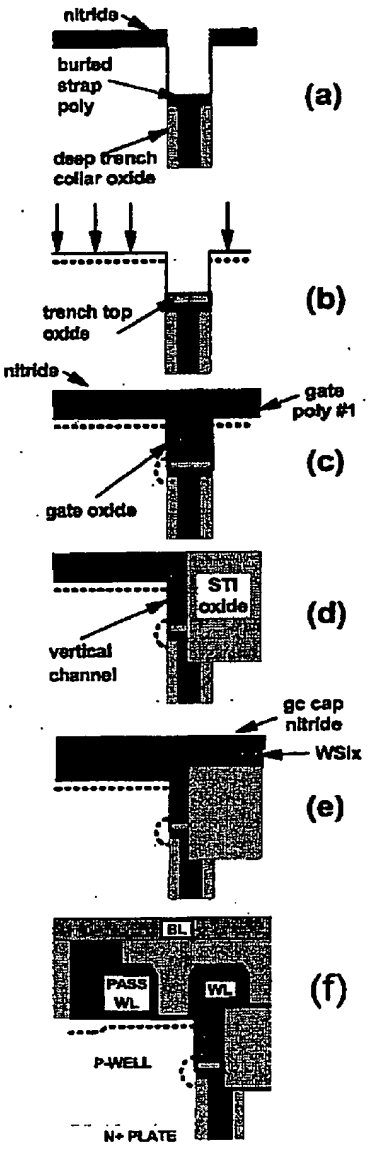

Fig.4: Key process steps for the formation of the vertical MOSFET.

TABLE I
Summary for key process steps corresponding to Fig. 4

(a)	STORAGE TRENCH and BURIED-STRAP CONNECTION
(b)	TRENCH TOP OXIDE ISOLATION and WELL and N^+ ARRAY JCT IMPLANTS
(c)	GATE OXIDATION and GATE POLY #1 DEPOSITION

along the exposed portions of the trench sidewall, and covered with a first gate polysilicon layer (Fig. 4c). Then isolation trenches are etched to a depth below the buried strap and filled with oxide, ensuring the isolation of the storage trenches and defining the edges of the vertical device (Fig. 4d and layout in Fig. 5). After depositing a poly/WSi_x/SiN layer (Fig. 4e) onto the first gate polysilicon layer, the gate conductors are patterned and etched simultaneously in the array and planar support device regions. Then conventional source/drain and self-aligned contact processing is used to